

CLAIMS

What is claimed is:

- 1 1. An apparatus comprising:
2 a differential amplifier, the differential amplifier having a first input coupled
3 to receive a voltage reference signal, a second input and an output;
4 an inverter, the inverter input coupled to the differential amplifier output,
5 wherein the inverter includes first and second transistors, the first and second
6 transistors having source/drain regions; and
7 a third transistor coupled between a source/drain region of the inverter and a
8 power supply rail to cause a switching point of the inverter to track a common mode
9 bias voltage of the differential amplifier.

- 1 2. The apparatus of claim 1, wherein the differential amplifier is a self-biased
2 amplifier.

- 1 3. The apparatus of claim 1, wherein a first source/drain region of the third
2 transistor is coupled to the source/drain region of the inverter and a second
3 source/drain region of the third transistor is coupled to the power supply rail, and
4 wherein a gate region of the third transistor is coupled to receive the voltage
5 reference signal.

- 1 4. The apparatus of claim 3, wherein the gate region of the third transistor is
2 coupled to a voltage scaling circuit to receive a voltage proportional to the voltage
3 reference signal.

- 1 5. The apparatus of claim 4, wherein the scaling circuit is an impedance divider
2 circuit.

1 6. The apparatus of claim 5, wherein the impedance divider circuit is a resistive
2 divider circuit.

1 7. The apparatus of claim 5, wherein the impedance divider circuit is a
2 capacitive divider circuit.

1 8. The apparatus of claim 2, wherein the differential amplifier includes:
2 an NMOS transistor differential input pair, wherein gate regions of the
3 differential input pair are coupled to the amplifier first and second inputs;
4 a PMOS transistor current mirror pair coupled as loads to first source/drain
5 regions of the differential input pair and coupled to a higher voltage supply rail; and
6 an NMOS tail transistor, a first source/drain region of the tail transistor
7 coupled to second source/drain regions of the differential input pair, a second
8 source/drain region of the tail transistor coupled to a lower voltage supply rail and a
9 gate region of the tail transistor coupled to gate regions of the current mirror pair.

1 9. The apparatus of claim 8, wherein the third transistor is an NMOS transistor
2 and is coupled to the lower voltage supply rail.

1 10. The apparatus of claim 2, wherein the differential amplifier includes:
2 a PMOS transistor differential input pair, wherein gate regions of the
3 differential input pair are coupled to the amplifier first and second inputs;
4 an NMOS transistor current mirror pair coupled as loads to first source/drain
5 regions of the differential input pair and coupled to a lower voltage supply rail; and
6 a PMOS tail transistor, a first source/drain region of the tail transistor
7 coupled to second source/drain regions of the differential input pair, a second
8 source/drain region of the tail transistor coupled to a higher voltage supply rail and a
9 gate region of the tail transistor coupled to gate regions of the current mirror pair.

1 11. The apparatus of claim 10, wherein the third transistor is a PMOS transistor
2 and is coupled to the higher voltage supply rail.

1 12. The apparatus of claim 1, wherein the apparatus is an input signal buffer
2 circuit, and wherein an input signal is applied to the second input of a differential
3 amplifier to cause the amplifier to switch output states as the input signal
4 approaches the voltage reference signal.

1 13. The apparatus of claim 1, wherein the reference voltage is within a range
2 including 0.6 volts to one volt.

1 14. The apparatus of claim 1, wherein the difference between a lower voltage
2 supply rail and a higher voltage supply rail is within a range including 1.05 volts to
3 1.8 volts.

1 15. The apparatus of claim 1, wherein the difference between a lower voltage
2 supply rail and a higher voltage supply rail is about three volts.

1 16. A method comprising:
2 applying a reference signal voltage to a first input of a differential input
3 amplifier, the differential amplifier having a common mode bias voltage and the
4 output of the differential amplifier coupled to an input of an inverter;
5 applying an input signal to a second input of a differential amplifier, the
6 input signal causing the differential amplifier to switch output states as an input
7 signal voltage approaches the reference signal voltage; and
8 adjusting the switching point of the inverter to track the common mode bias
9 voltage of the differential amplifier by coupling the reference signal voltage to a
10 gate region of a tail transistor connected in series between the inverter and a power
11 supply rail.

1 17. The method of claim 16, wherein coupling the reference signal voltage to a
2 gate region of a tail transistor includes coupling a voltage proportional to the
3 reference signal voltage to the gate region of the tail transistor.

1 18. The method of claim 17, wherein applying a reference signal voltage
2 includes changing the reference signal voltage if a voltage difference between a
3 higher voltage supply rail and a lower voltage supply rail changes.

1 19. The method of claim 18, wherein coupling a voltage proportional to the
2 reference signal voltage includes changing the proportional voltage if the voltage
3 difference between the higher and lower supply rails changes.

1 20. A system comprising:
2 a first integrated circuit;
3 a second integrated circuit, the second integrated circuit including a plurality
4 of interface circuits coupled to the first integrated circuit, an interface circuit
5 including:
6 a differential amplifier, the differential amplifier having a first input
7 coupled to receive a voltage reference signal, a second input and an output;
8 an inverter, the inverter input coupled to the differential amplifier
9 output, wherein the inverter includes first and second transistors, the first
10 and second transistors having source/drain regions; and
11 a third transistor coupled between the inverter and a power supply rail such
12 that a first source/drain region of the third transistor is coupled to a source/drain
13 region of the inverter and a second source/drain region of the third transistor is
14 coupled to the power supply rail, and wherein a gate region of the third transistor is
15 coupled to receive the voltage reference signal.

1 21. The system of claim 20, wherein the voltage reference is scalable to adjust
2 the reference in response to a change in a high voltage power supply rail of the first
3 integrated circuit.

1 22. The system of claim 21, wherein a difference between a higher voltage
2 supply rail and a lower voltage supply rail on the first integrated circuit is unequal to
3 a difference between a difference between a higher voltage supply rail and a lower
4 voltage supply rail on the second integrated circuit.

1 23. The system of claim 20, wherein the first and second integrated circuits are
2 included in a memory controller.

1 24. The system of claim 20, wherein the first integrated circuit includes a
2 processor.

1 25. A computer system comprising:
2 a DRAM;
3 a memory controller coupled to the DRAM; and
4 a processor coupled to the memory controller, the processor to process
5 information, the processor and the memory controller communicating through
6 interface circuits, an interface circuit including:
7 a differential amplifier, the differential amplifier having a first input
8 coupled to receive a voltage reference signal, a second input and an output;
9 an inverter, the inverter input coupled to the differential amplifier
10 output, wherein the inverter includes first and second transistors, the first
11 and second transistors having source/drain regions; and
12 a third transistor coupled between a source/drain region of the inverter and a
13 power supply rail to cause a switching point of the inverter to track a common mode
14 bias voltage of the differential amplifier.

1 26. The computer system of claim 25, wherein the differential amplifier is a self-
2 biased amplifier.

1 27. The computer system of claim 25, wherein the third transistor is coupled
2 between the inverter and a power supply rail such that a first source/drain region of
3 the third transistor is coupled to a source/drain region of the inverter and a second
4 source/drain region of the third transistor is coupled to the power supply rail, and
5 wherein a gate region of the third transistor is coupled to receive the voltage
6 reference signal.